SREE VIDYANIKETHAN ENGINEERING COLLEGE
(AUTONOMOUS)
Sree Sainath Nagar, A. Rangampet – 517 102

SVEC/EC/2011-12/A-305

12.09.2011

CIRCULAR

All the M. Tech. II Semester students are informed that the II- Mid-Term examinations will be conducted as per the schedule shown below.

DATE /DAY	TIME	Electrical Power Systems (EPS)	Computer Science (CS)	Digital Electronics and Communication Systems (DECS)	VLSI	Software Engineering(SE)	Bio-Technology
26/09/11 MON	2.30 PM TO 4.30 PM	Economic Operation & Control of Power System	Computer Networks	Adaptive Signal Processing	Algorithms for VLSI Physical Design Automation	Service oriented Architecture	Bioreactor Engineering
27/09/11 TUE	2.30 PM TO 4.30 PM	FACTS Controllers	Data Warehousing and Data mining	Coding Theory and Techniques	CPLD & FPGA Architectures and Applications	Software Architecture and Design patterns	Genetic Engineering
28/09/11 WED	2.30 PM TO 4.30 PM	HVDC Transmission	JAVA and Web Technologies	Detection and Estimation of Signals	Digital System Testing and Testability	Software Reengineering and Reuse	Bioseparation Processes
29/09/11 THU	2.30 PM TO 4.30 PM	Power System Reliability	Object Oriented Analysis and Design	High Performance Networks	Low Power VLSI Design	Software Security Engineering	Cell Technology
30/09/11 FRI	2.30 PM TO 4.30 PM	Static and Digital Protection of Power System	Operating Systems	Wireless Communications	Scripting Language for VLSI Design Automation	Software Quality Assurance and Testing	Bioinformatics
01/10/11 SAT	2.30 PM TO 4.30 PM	Energy Audit, Conservation & Management	System Thinking	Optical Communications	Nano Electronics	Information Retrieval Systems	Advanced Immunotechnology

PRINCIPAL

Copy to: 1) The HODs of EEE, ECE, CSE , IT & BOT with a request to circulate among the students and staff and display on the department notice board.
2) Director, PG Courses
3) The Examination Section
4) A.O, for necessary transport arrangement.