Sree Vidyanikethan Engineering College (Autonomous)

Sree Sainath Nagar, A. Rangampet, Tirupati,Chittoor,Andhra Pradesh

Polytechnic Diploma VI Semester (C-14) Unit Test - I Examinations January 2017

TIME - TABLE

Date : 21/12/2016

Time : 03:00 PM TO 04:00 PM

EXAM DATE & TIME	WEEK DAY	DIPLOMA-DCE	DIPLOMA-DCME	DIPLOMA-DECE	DIPLOMA-DEEE	DIPLOMA-DME
04/01/2017 3:00PM TO 4:00PM	WEDNESDAY	STEEL STRUCTURES [C601]	INDUSTRIALMANAGEMENT& ENTREPRENEURSHIP [CM601]	INDUSTRIAL MANAGEMENT [EC601]	INDUSTRIAL MANAGEMENT [EE601]	ENTREPREURSHIP AND PROJECT MANAGEMENT [M601]
05/01/2017 3:00PM TO 4:00PM	THURSDAY	ENVIRONMENTAL ENGINEERING - II [C602]	ADVANCE JAVA PROGRAMMING [CM602]	INDUSTRIAL ELECTRONICS [EC602]	ELECTRIC TRACTION [EE602]	REFRIGERATION&AIR CONDITOIONING [M602]
06/01/2017 3:00PM TO 4:00PM	FRIDAY	CONSTRUCTION TECHNOLOGY AND [C603]	SYSTEM ADMINISTRATION [CM603]	ELECTRONIC CIRCUIT DESIGN @QUALITY [EC603]	POWER SYSTEMS 3 (SGP) [EE603]	ENERGY SOURCES AND POWER PLANT [ME603]
09/01/2017 3:00PM TO 4:00PM	MONDAY	CONSTRUCTION FAILURES&REPAIRS AND [C604]	MOBILE COMMUNICATION [CM604]	MOBILE COMMUNICATIONS [EC604]	POWER ELECTRONICS [EE604]	COMPUTER AIDED MANUFACTURING [M604]
10/01/2017 3:00PM TO 4:00PM	TUESDAY	QUALITY CONTROL & SAFETY IN CONSTRUCTION [C605]	.NET PROGRAMMING [CM605]	ADVANCED MICROCONTROLLERS & DSP [EC605]	MICRO CONTROLLER AND APPLICATIONS [EE605]	MEASUREMENT & CONTROL SYSTEMS [M605]
11/01/2017 3:00PM TO 4:00PM	WEDNESDAY	--	CRYPTOGRAPHY AND NETWORK SECURITY [CM606]	DIGITAL CIRCUIT DESIGN THROUGH VERILOG HDL [EC606]	INDUSTRIAL AUTOMATION [EE606]	AUTOMOBILE ENGINEERING [M606]

PRINCIPAL

Copy to: 1) The Director, SVEC

2) The Vice Principal, 2nd Shift Polytechnic: With a request to arrange to read out in the respective classes and to display on the Notice Board

3) S.A.O. for Information

4) The Exam Section

5) Notice Board