## **Sree Vidyanikethan Engineering College (Autonomous)**

## Sree Sainath Nagar, A. Rangampet, Tirupati, Chittoor, Andhra Pradesh M.Tech I Semester (SVEC-14) Supplementary Examinations, August 2017

## TIME - TABLE

Date: 24/06/2017

Time: 10:00 AM TO 01:00 PM

EXAM DATE & TIME	WEEK DAY	MTECH-CMS	MTECH-CNIS	MTECH-CS	MTECH-DECS	MTECH-EPS	MTECH-SE	MTECH-VLSI
17/08/2017 10:00AM TO 1:00PM	THURSDAY	ADVANCED DIGITAL SIGNAL PROCESSING	ADVANCED COMPUTER NETWORKS	ADVANCED COMPUTER NETWORKS	COMPUTER ARCHITECTURES	POWER SYSTEM SECURITY AND STATE ESTIMATION	SOFTWARE DEVELOPMENT METHODOLOGIES	ANALOG IC DESIGN
		[14MT15706]	[14MT10501]	[14MT10501]	[14MT13801]	[14MT10701]	[14MT12501]	[14MT15701]
19/08/2017 10:00AM TO 1:00PM	SATURDAY	DIGITAL COMMUNICATION TECHNIQUES	INFORMATION SECURITY	ADVANCED DATABASE MANAGEMENT SYSTEMS	DIGITAL COMMUNICATION TECHNIQUES	STATIC AND DIGITAL PROTECTION OF POWER SYSTEM	SOFTWARE PROCESS AND PROJECT MANAGEMENT	COMPUTATIONAL TECHNIQUES IN MICROELECTRONICS
		[14MT13802]	[14MT20507]	[14MT10502]	[14MT13802]	[14MT10702]	[14MT12502]	[14MT15702]
22/08/2017 10:00AM TO 1:00PM	TUESDAY	COMPUTER NETWORKS	MOBILE COMPUTING	ADVANCED SOFTWARE ENGINEERING	DIGITAL SYSTEM DESIGN	ADVANCED POWER SYSTEM STABILITY ANALYSIS	SOFTWARE REQUIREMENTS AND ESTIMATION	DEVICE MODELING
		[14MT13805]	[14MT20508]	[14MT10503]	[14MT13803]	[14MT10703]	[14MT12503]	[14MT15703]
24/08/2017 10:00AM TO 1:00PM	THURSDAY	LINEAR ALGEBRA	NETWORK MANAGEMENT	DATA STRUCTURES AND ALGORITHMS	LINEAR ALGEBRA	POWER ELECTRONIC CONVERTERS	DATA STRUCTURES AND ALGORITHMS	DIGITAL IC DESIGN
		[14MT13809]	[14MT16301]	[14MT10504]	[14MT13809]	[14MT10704]	[14MT10504]	[14MT15704]
28/08/2017 10:00AM TO 1:00PM	MONDAY	OPTICAL COMMUNICATIONS AND NETWORKS	WIRELESS NETWORKS	DISCRETE STRUCTURES AND GRAPH THEORY	MODERN DIGITAL SIGNAL PROCESSING	ADVANCED CONTROL SYSTEMS	WEB TECHNOLOGIES	IC FABRICATION
		[14MT23808]	[14MT16302]	[14MT10505]	[14MT13804]	[14MT10705]	[14MT12504]	[14MT15705]
30/08/2017 10:00AM TO 1:00PM	WEDNESDAY	SATELLITE COMMUNICATIONS	DATA WAREHOUSING AND DATA MINING	SOFTWARE PROJECT MANAGEMENT	EMBEDDED SYSTEM DESIGN	REACTIVE POWER COMPENSATION AND MANAGEMENT	CLOUD COMPUTING	LOW VOLTAGE ANALOG CIRCUIT DESIGN
		[14MT16102]	[14MT20503]	[14MT10509]	[14MT13807]	[14MT10707]	[14MT12508]	[14MT15708]
01/09/2017 10:00AM TO 1:00PM	FRIDAY	RESEARCH	RESEARCH .	RESEARCH	RESEARCH	RESEARCH	RESEARCH	RESEARCH METHODOLOGY
		METHODOLOGY [14MT10310]	METHODOLOGY [14MT10310]	METHODOLOGY [14MT10310]	METHODOLOGY [14MT10310]	METHODOLOGY [14MT10310]	METHODOLOGY [14MT10310]	[14MT10310]

- 1. Students have to bring their College Identity Cards to the examination hall; otherwise they will not be permitted to write the examination.
- 2. Examination will be on the Units prescribed in the Syllabus Book.
- 3. College buses will leave the college with in 15 minutes after Examination Time.

Copy to:

1) The Director, SVEC.

- 2) The HODs of EEE, ECE, CSE & IT: with a request to arrange to read out in the respective class rooms and circulation among the staff and to display on notice board.
- 3) The Examination Section.
- 4) The S.A.O, for information and necessary transport arrangement.