Sree Vidyanikethan Engineering College (Autonomous)

Sree Sainath Nagar, A. Rangampet, Tirupati,Chittoor,Andhra Pradesh

M.Tech II Semester (SVEC-16) Supplementary Examinations, October 2018

TIME - TABLE

Date : 11/09/2018

Time : 02:00 PM TO 05:00 PM

EXAM DATE & TIME	WEEK DAY	MTECH-CMS	MTECH-CNIS	MTECH-CS	MTECH-DECS	MTECH-EPS	MTECH-SE	MTECH-VLSI
29/10/2018 2:00PM TO 5:00PM	MONDAY	DETECTION AND ESTIMATION OF SIGNALS [16MT23801]	INTRUSION DETECTION SYSTEMS [16MT26301]	ADVANCED COMPUTER ARCHITECTURE [16MT20501]	DETECTION AND ESTIMATION OF SIGNALS [16MT23801]	FLEXIBLE AC TRANSMISSION SYSTEM [16MT20701]	BIG DATA TECHNOLOGIES [16MT22501]	LOW POWER VLSI DESIGN [16MT25701]
31/10/2018 2:00PM TO 5:00PM	WEDNESDAY	ADAPTIVE SIGNAL PROCESSING [16MT26101]	BIG DATA ANALYTICS [16MT20502]	BIG DATA ANALYTICS [16MT20502]	EMBEDDED SYSTEM DESIGN [16MT23802]	INTELLIGENT SYSTEMS [16MT20702]	SERVICE ORIENTED ARCHITECTURE [16MT22502]	MIXED SIGNAL DESIGN [16MT25702]
02/11/2018 2:00PM TO 5:00PM	FRIDAY	IMAGE & VIDEO PROCESSING [16MT13804]	NETWORK PROGRAMMING [16MT26302]	OBJECT ORIENTED ANALYSIS AND DESIGN [16MT20503]	INFORMATION THEORY AND CODING TECHNIQUES [16MT23803]	POWER SYSTEM STABILITY AND CONTROL [16MT20703]	SOFTWARE ARCHITECTURE & DESIGN PATTERNS [16MT22503]	NANOELECTRONICS [16MT25703]
06/11/2018 2:00PM TO 5:00PM	TUESDAY	SMART ANTENNAS [16MT26102]	CLOUD COMPUTING [16MT12501]	CLOUD COMPUTING [16MT12501]	LOW POWER CMOS VLSI DESIGN [16MT23804]	RESTRUCTURED POWER SYSTEM [16MT20704]	SOFTWARE TESTING TECHNIQUES [16MT22504]	PHYSICAL DESIGN AUTOMATION [16MT25704]
09/11/2018 2:00PM TO 5:00PM	FRIDAY	WIRELESS COMMUNICATIONS [16MT23805]	WIRELESS NETWORKS [16MT26303]	WEB TECHNOLOGIES [16MT22505]	WIRELESS COMMUNICATIONS [16MT23805]	STATIC AND DIGITAL PROTECTION OF POWER SYSTEM [16MT20705]	WEB TECHNOLOGIES [16MT22505]	TESTING AND TESTABILITY [16MT25705]
12/11/2018 2:00PM TO 5:00PM	MONDAY	RADAR SIGNAL PROCESSING [16MT26104]	COMPUTER FORENSICS [16MT26304]	MOBILE COMPUTING [16MT20506]	OPTICAL COMMUNICATIONS AND NETWORKS [16MT23807]	POWER QUALITY [16MT20708]	SOFTWARE PROCESS AND PROJECT MANAGEMENT [16MT22506]	SYSTEM-ON-CHIP DESIGN AND VERIFICATION [16MT25708]

CHIEF CONTROLLER OF EXAMINATIONS

Copy to: 1) The Director, SVEC.

2) The HODs of EEE, ECE, CSE & IT: with a request to arrange to read out in the respective class rooms and circulation among the staff and to display on notice board.

3) The Examination Section.

4) The S.A.O, for information and necessary transport arrangement.