Sree Vidyanikethan Engineering College (Autonomous)

Sree Sainath Nagar, A. Rangampet, Tirupati, Chittoor, Andhra Pradesh

M.Tech I Semester (SVEC-16) Supplementary Examinations, October 2018

TIME - TABLE

Date: 11/09/2018

Time: 02:00 PM TO 05:00 PM

CHIEF CONTROLLER OF EXAMINATIONS

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EXAM DATE & TIME	WEEK DAY	MTECH-CMS	MTECH-CS	MTECH-DECS	MTECH-EPS	MTECH-PED	MTECH-VLSI
30/10/2018 2:00PM TO 5:00PM	TUESDAY	ADVANCED DIGITAL SIGNAL PROCESSING	ADVANCED COMPUTER NETWORKS	COMPUTER NETWORKS	ADVANCED CONTROL SYSTEMS	APPLIED MATHEMATICS	ANALOG IC DESIGN
		[16MT15706]	[16MT10501]	[16MT13801]	[16MT10701]	[16MT1BS01]	[16MT15701]
01/11/2018 2:00PM TO 5:00PM	THURSDAY	DIGITAL COMMUNICATION TECHNIQUES	ADVANCED DATABASE MANAGEMENT SYSTEMS	DIGITAL COMMUNICATION TECHNIQUES	HIGH VOLTAGE ENGINEERING	ADVANCED POWER SEMICONDUCTOR DEVICES	COMPUTATIONAL METHODS IN MICROELECTRONICS
		[16MT13802]	[16MT10502]	[16MT13802]	[16MT10702]	[16MT18301]	[16MT15702]
05/11/2018 2:00PM TO 5:00PM	MONDAY	INFORMATION THEORY AND CODING TECHNIQUES	ADVANCED OPERATING SYSTEMS	DIGITAL SYSTEM DESIGN AND TESTING	POWER ELECTRONIC CONVERTERS	ANALYSIS OF INVERTERS	DEVICE MODELING
		[16MT23803]	[16MT10503]	[16MT13803]	[16MT10703]	[16MT18302]	[16MT15703]
08/11/2018 2:00PM TO 5:00PM	THURSDAY	OPTICAL COMMUNICATIONS AND NETWORKS	DATA WAREHOUSING AND DATA MINING	IMAGE & VIDEO PROCESSING	POWER SYSTEM SECURITY AND STATE ESTIMATION	ANALYSIS OF POWER CONVERTERS	DIGITAL IC DESIGN
		[16MT23807]	[16MT10504]	[16MT13804]	[16MT10704]	[16MT18303]	[16MT15704]
10/11/2018 2:00PM TO 5:00PM	SATURDAY	RF CIRCUIT DESIGN	DATA STRUCTURES AND ALGORITHMS	MODERN DIGITAL SIGNAL PROCESSING	REACTIVE POWER COMPENSATION AND MANAGEMENT	MODELLING OF ELECTRICAL MACHINES	IC FABRICATION
		[16MT16101]	[16MT12502]	[16MT13805]	[16MT10705]	[16MT18304]	[16MT15705]
13/11/2018 2:00PM TO 5:00PM	TUESDAY	DIGITAL SATELLITE COMMUNICATIONS	SOFTWARE TESTING TECHNIQUES	ASIC DESIGN	MICROCONTROLLERS AND APPLICATIONS	MICROCONTROLLERS AND APPLICATIONS	REAL TIME SYSTEMS
		[16MT16102]	[16MT22504]	[16MT13806]	[16MT10707], POWER SYSTEM RELIABILITY	[16MT10707]	[16MT23808]
					[16MT10708]	*	

Copy to: 1) The Director, SVEC.

2) The HODs of EEE, ECE, CSE & IT: with a request to arrange to read out in the respective class rooms and dirculation among the staff and to display on notice board.

3) The Examination Section.

4) The S.A.O, for information and necessary transport arrangement.