

SREE VIDYANIKETHAN ENGINEERING COLLEGE (AUTONOMOUS)

Sree Sainath Nagar, A. Rangampet, Tirupati, Chittoor, Andhra Pradesh

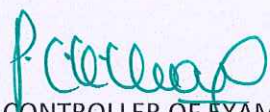
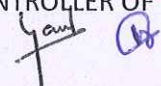
M.Tech I Semester (SVEC-16) Regular Examinations, January 2019

TIME - TABLE

Date : 28/11/2018

Time : 02:00 PM TO 05:00 PM

EXAM DATE & TIME	WEEK DAY	MTECH-CS	MTECH-EPS	MTECH-VLSI
21/01/2019 2:00PM TO 5:00PM	MONDAY	ADVANCED COMPUTER NETWORKS [16MT10501]	ADVANCED CONTROL SYSTEMS [16MT10701]	ANALOG IC DESIGN [16MT15701]
23/01/2019 2:00PM TO 5:00PM	WEDNESDAY	ADVANCED DATABASE MANAGEMENT SYSTEMS [16MT10502]	HIGH VOLTAGE ENGINEERING [16MT10702]	COMPUTATIONAL METHODS IN MICROELECTRONICS [16MT15702]
25/01/2019 2:00PM TO 5:00PM	FRIDAY	ADVANCED OPERATING SYSTEMS [16MT10503]	POWER ELECTRONIC CONVERTERS [16MT10703]	DEVICE MODELING [16MT15703]
29/01/2019 2:00PM TO 5:00PM	TUESDAY	DATA WAREHOUSING AND DATA MINING [16MT10504]	POWER SYSTEM SECURITY AND STATE ESTIMATION [16MT10704]	DIGITAL IC DESIGN [16MT15704]
31/01/2019 2:00PM TO 5:00PM	THURSDAY	DATA STRUCTURES AND ALGORITHMS [16MT12502]	REACTIVE POWER COMPENSATION AND MANAGEMENT [16MT10705]	IC FABRICATION [16MT15705]
04/02/2019 2:00PM TO 5:00PM	MONDAY	SOFTWARE TESTING TECHNIQUES [16MT22504]	MICROCONTROLLERS AND APPLICATIONS [16MT10707]	FPGA ARCHITECTURES AND APPLICATIONS. [16MT15707]


CHIEF CONTROLLER OF EXAMINATIONS


Copy to: 1) The Director, SVEC.

- 2) The HODs of EEE, ECE & CSE: with a request to arrange to read out in the respective class rooms and circulation among the staff and to display on notice board.
- 3) The Examination Section.
- 4) The S.A.O, for information and necessary transport arrangement.