Sree Vidyanikethan Engineering College (Autonomous)

Sree Sainath Nagar, A. Rangampet, Tirupati, Chittoor, Andhra Pradesh M.Tech Il Semester (SVEC-16) Supplementary Examinations ,January 2019 TIME - TABLE

Date: 05/12/2018

Time: 02:00 PM TO 05:00 PM

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EXAM DATE & TIME	WEEK DAY	MTECH-CMS	MTECH-CNIS	MTECH-CS	MTECH-DECS	MTECH-EPS	MTECH-PED	MTECH-SE	MTECH-VLSI
22/01/2019 2:00PM TO 5:00PM	TUESDAY	DETECTION AND ESTIMATION OF SIGNALS [16MT23801]	INTRUSION DETECTION SYSTEMS [16MT26301]	ADVANCED COMPUTER ARCHITECTURE [16MT20501]	DETECTION AND ESTIMATION OF SIGNALS [16MT23801]	FLEXIBLE AC TRANSMISSION SYSTEM [16MT20701]	LINEAR AND NONLINEAR CONTROL SYSTEMS [16MT28301]	BIG DATA TECHNOLOGIES [16MT22501]	LOW POWER VLSI DESIGN [16MT25701]
24/01/2019 2:00PM TO 5:00PM	THURSDAY	ADAPTIVE SIGNAL PROCESSING	BIG DATA ANALYTICS [16MT20502]	BIG DATA ANALYTICS [16MT20502]	EMBEDDED SYSTEM DESIGN [16MT23802]	INTELLIGENT SYSTEMS [16MT20702]	POWER ELECTRONICS IN RENEWABLE ENERGY SYSTEMS [16MT28302]	SERVICE ORIENTED ARCHITECTURE [16MT22502]	MIXED SIGNAL DESIGN [16MT25702]
28/01/2019 2:00PM TO 5:00PM	MONDAY	IMAGE & VIDEO PROCESSING	NETWORK PROGRAMMING	OBJECT ORIENTED ANALYSIS AND DESIGN	INFORMATION THEORY AND CODING TECHNIQUES	POWER SYSTEM STABILITY AND CONTROL	SOLID STATE AC DRIVES	SOFTWARE ARCHITECTURE & DESIGN PATTERNS	NANOELECTRONIC
		[16MT13804]	[16MT26302]	[16MT20503]	[16MT23803]	[16MT20703]	[16MT28303]	[16MT22503]	[16MT25703]
30/01/2019 2:00PM TO 5:00PM	WEDNESDAY	SMART ANTENNAS	CLOUD COMPUTING	CLOUD COMPUTING	LOW POWER CMOS VLSI DESIGN	RESTRUCTURED POWER SYSTEM	SOLID STATE DC DRIVES	SOFTWARE TESTING TECHNIQUES	PHYSICAL DESIGN AUTOMATION
		[16MT26102]	[16MT12501]	[16MT12501]	[16MT23804]	[16MT20704]	[16MT28304]	[16MT22504]	[16MT25704]
01/02/2019 2:00PM TO 5:00PM	FRIDAY	WIRELESS COMMUNICATIONS	WIRELESS NETWORKS	WEB TECHNOLOGIES	WIRELESS COMMUNICATIONS	STATIC AND DIGITAL PROTECTION OF POWER SYSTEM	SPECIAL ELECTRICAL MACHINES	WEB TECHNOLOGIES	TESTING AND TESTABILITY
		[16MT23805]	[16MT26303]	[16MT22505]	[16MT23805]	[16MT20705]	[16MT28305]	[16MT22505]	[16MT25705]
05/02/2019 2:00PM TO 5:00PM		RADAR SIGNAL PROCESSING	COMPUTER FORENSICS	INFORMATION SECURITY	OPTICAL COMMUNICATIONS AND NETWORKS	POWER QUALITY	POWER QUALITY	SOFTWARE PROCESS AND PROJECT MANAGEMENT	SYSTEM-ON-CHIP DESIGN AND VERIFICATION
	TUESDAY	[16MT26104] ,WIRELESS SENSOR NETWORKS [16MT25709]	[16MT26304]	· [16MT20505] ,MOBILE COMPUTING [16MT20506]	[16MT23807]	[16MT20708]	[16MT20708]	[16MT22506]	[16MT25708]

CHIEF CONTROLLER OF EXAMINATIONS

Copy to: 1) The Director, SVEC.
2) The HODs of EEE, ECE, CSE & IT: with a request to arrange to read out in the respective class rooms and circulation among the staff and to display on notice board.

- 3) The Examination Section.
- 4) The S.A.O, for information and necessary transport arrangement.