Sree Vidyanikethan Engineering College (Autonomous)

Sree Sainath Nagar, A. Rangampet, Tirupati,Chittoor,Andhra Pradesh

M.Tech I Semester (SVEC 16) Mid-II Examinations, December 2018

TIME - TABLE

Date : 17/12/2018

Time : 09:30 AM TO 11:30 AM

EXAM DATE & TIME	WEEK DAY	MTECH-CS	MTECH-EPS	MTECH-VLSI
31/12/2018 9:30AM TO 11:30AM	MONDAY	ADVANCED COMPUTER NETWORKS [16MT10501]	ADVANCED CONTROL SYSTEMS [16MT10701]	ANALOG IC DESIGN [16MT15701]
01/01/2019 9:30AM TO 11:30AM	TUESDAY	ADVANCED DATABASE MANAGEMENT SYSTEMS [16MT10502]	HIGH VOLTAGE ENGINEERING [16MT10702]	COMPUTATIONAL METHODS IN MICROELECTRONICS [16MT15702]
02/01/2019 9:30AM TO 11:30AM	WEDNESDAY	ADVANCED OPERATING SYSTEMS [16MT10503]	POWER ELECTRONIC CONVERTERS [16MT10703]	DEVICE MODELING [16MT15703]
03/01/2019 9:30AM TO 11:30AM	THURSDAY	DATA WAREHOUSING AND DATA MINING [16MT10504]	POWER SYSTEM SECURITY AND STATE ESTIMATION [16MT10704]	DIGITAL IC DESIGN [16MT15704]
04/01/2019 9:30AM TO 11:30AM	FRIDAY	DATA STRUCTURES AND ALGORITHMS [16MT12502]	REACTIVE POWER COMPENSATION AND MANAGEMENT [16MT10705]	IC FABRICATION [16MT15705]
07/01/2019 9:30AM TO 11:30AM	MONDAY	SOFTWARE TESTING TECHNIQUES [16MT22504]	MICROCONTROLLERS AND APPLICATIONS [16MT10707]	FPGA ARCHITECTURES AND APPLICATIONS [16MT15707]

1. Students have to bring their College Identity Cards to the examination hall; otherwise they will not be permitted to write the examination.
2. Examination will be on the Units prescribed in the Syllabus Book.
3. College buses will leave the college with in 15 minutes after Examination Time.

PRINCIPAL

Copy to: 1) The Director, SVEC.
2) The HODs of EEE, ECE & CSE : with a request to arrange to read out in the respective class rooms and circulation among the staff and to display on notice board.
3) The Examination Section.
4) The S.A.O, for information and necessary transport arrangement.