

Sree Vidyanikethan Engineering College (Autonomous)

Sree Sainath Nagar, A. Rangampet, Tirupati, Chittoor, Andhra Pradesh

M.Tech I Semester (SVEC 19) Mid-I Examinations, November 2019

TIME - TABLE

Date : 11/11/2019

Time : 02:45 PM TO 04:45 PM

EXAM DATE & TIME	WEEK DAY	MTECH-CS	MTECH-EPS	MTECH-VLSI	MTECH-PED
25/11/2019 2:45PM TO 4:45PM	MONDAY	Advanced Algorithms 19MT10501	High Voltage Engineering 19MT10701	Analog CMOS VLSI Design 19MT15701	Dynamics of Electrical Machines 19MT18301
26/11/2019 2:45PM TO 4:45PM	TUESDAY	Advanced Data Structures 19MT10502	Power Electronics for Power Systems 19MT10702	Device Modeling 19MT15702	Power Electronic Converters 19MT18302
27/11/2019 2:45PM TO 4:45PM	WEDNESDAY	Mathematical Foundations of Computer Science 19MT10503	Power System Security and State Estimation 19MT10703	Digital CMOS VLSI Design 19MT15703	Power Semiconductor Devices and Modeling 19MT18303
28/11/2019 2:45PM TO 4:45PM	THURSDAY	Data Warehousing and Data Mining 19MT10505	Intelligent Controllers 19MT18305	IC Fabrication 19MT15705	Intelligent Controllers 19MT18305
29/11/2019 2:45PM TO 4:45PM	FRIDAY	Cloud Computing 19MT16303	Power Quality 19MT10706	Mixed Signal Design 19MT15709	Power Quality 19MT10706
30/11/2019 2:45PM TO 4:45PM	SATURDAY	Research Methodology and IPR 19MT10708	Research Methodology and IPR 19MT10708	Research Methodology and IPR 19MT10708	Research Methodology and IPR 19MT10708

1. Students have to bring their College Identity Cards to the examination hall; otherwise they will not be permitted to write the examination.
2. Examination will be on the Units prescribed in the Syllabus Book.
3. College buses will leave the college with in 15 minutes after Examination Time.

- Copy to:
1. The Director, SVEC.
 2. The Dean Academics, SVEC.
 3. The Vice-Principal, SVEC.
 4. The HODs of EEE, ECE & CSE : with a request to arrange to read out in the respective class rooms and circulation among the staff and to display on notice board.
 5. The Examination Section.
 6. The S.A.O, for information and necessary transport arrangement.


PRINCIPAL
