Sree Vidyanikethan Engineering College (Autonomous)

Sree Sainath Nagar, A. Rangampet, Tirupati,Chittoor,Andhra Pradesh

M.Tech I Semester (SVEC-19) Supplementary Examinations, January 2022

TIME - TABLE

Date : 07.12.2021

Time : 02:00 PM TO 05:00 PM

EXAM DATE & TIME	WEEK DAY	MTECH-CS	MTECH-EPS	MTECH-PED	MTECH-VLSI
07/01/2022 2:00 PM TO 5:00 PM	FRIDAY	ADVANCED ALGORITHMS **[19MT10501]**	HIGH VOLTAGE ENGINEERING **[19MT10701]**	DYNAMICS OF ELECTRICAL MACHINES **[19MT18301]**	ANALOG CMOS VLSI DESIGN **[19MT15701]**
10/01/2022 2:00 PM TO 5:00 PM	MONDAY	ADVANCED DATA STRUCTURES **[19MT10502]**	POWER ELECTRONICS FOR POWER SYSTEMS **[19MT10702]**	POWER ELECTRONIC CONVERTERS **[19MT18302]**	DEVICE MODELING **[19MT15702]**
12/01/2022 2:00 PM TO 5:00 PM	WEDNESDAY	MATHEMATICAL FOUNDATIONS OF COMPUTER SCIENCE **[19MT10503]**	POWER SYSTEM SECURITY AND STATE ESTIMATION **[19MT10703]**	POWER SEMICONDUCTOR DEVICES AND MODELING **[19MT18303]**	DIGITAL CMOS VLSI DESIGN **[19MT15703]**
18/01/2022 2:00 PM TO 5:00 PM	TUESDAY	DATA WAREHOUSING AND DATA MINING **[19MT10505]** WIRELESS SENSOR NETWORKS **[19MT26302]**	INTELLIGENT CONTROLLERS **[19MT18305]**	INTELLIGENT CONTROLLERS **[19MT18305]**	IC FABRICATION **[19MT15705]**
20/01/2022 2:00 PM TO 5:00 PM	THURSDAY	CLOUD COMPUTING **[19MT16303]**	POWER QUALITY **[19MT10706]**	POWER QUALITY **[19MT10706]**	MIXED SIGNAL DESIGN **[19MT15709]** FPGA ARCHITECTURES **[19MT15707]**
22/01/2022 2:00 PM TO 5:00 PM	SATURDAY	RESEARCH METHODOLOGY AND IPR **[19MT10708]**	RESEARCH METHODOLOGY AND IPR **[19MT10708]**	RESEARCH METHODOLOGY AND IPR **[19MT10708]**	RESEARCH METHODOLOGY AND IPR **[19MT10708]**

CHIEF CONTROLLER OF EXAMINATIONS

Copy to : The Director, Academics & Research, SVEC.
The Vice-Principal, SVEC
The Dean, Academics
The Dean, Placements
The HODs, of EEE, ECE & CSE : with a request to arrange to read over in the respective class rooms and circulate among the staff members and display on notice Board.
The Examination Section
The S.A.O, S.V.E.C
Hostel Notice Boards
The office, ISA.