Sree Vidyanikethan Engineering College (Autonomous)

Sree Sainath Nagar, A. Rangampet, Tirupati,Chittoor,Andhra Pradesh

M.Tech I Semester (SVEC 19) Regular Examinations, June 2022

TIME - TABLE

Date : 05/05/2022

Time : 02:00 PM TO 05:00 PM

EXAM DATE & TIME	WEEK DAY	MTECH-VLSI
01/06/2022 2:00 PM TO 5:00 PM	WEDNESDAY	Analog CMOS VLSI Design 19MT15701
03/06/2022 2:00 PM TO 5:00 PM	FRIDAY	Device Modeling 19MT15702
06/06/2022 2:00 PM TO 5:00 PM	MONDAY	Digital CMOS VLSI Design 19MT15703
08/06/2022 2:00 PM TO 5:00 PM	WEDNESDAY	IC Fabrication 19MT15705
10/06/2022 2:00 PM TO 5:00 PM	FRIDAY	FPGA Architectures 19MT15707
13/06/2022 2:00 PM TO 5:00 PM	MONDAY	Research Methodology and IPR 19MT10708

CHIEF CONTROLLER OF EXAMINATIONS

Copy to : The Director, Academics & Research,SVEC.
The Vice-Principal, SVEC.
The Dean, Academics,
The Dean, Placements,
The HOD of ECE : with a request to arrange to read over in the respective class rooms and circulate among the staff members and display on notice Board.
The Examination Section.
The S.A.O, SVEC.
Hostel Notice Boards.
The Office, ISA.