Sree Vidyanikethan Engineering College (Autonomous)

Sree Sainath Nagar, A. Rangampet, Tirupati,Chittoor,Andhra Pradesh

M.Tech I Semester (SVEC 19) Mid-II Examinations, May 2022

TIME - TABLE

Date : 09/05/2022

Time : 02:30 PM TO 04:30 PM

EXAM DATE & TIME	WEEK DAY	MTECH-VLSI
23/05/2022 2:30 PM TO 4:30 PM	MONDAY	Analog CMOS VLSI Design **19MT15701**
24/05/2022 2:30 PM TO 4:30 PM	TUESDAY	Device Modeling **19MT15702**
25/05/2022 2:30 PM TO 4:30 PM	WEDNESDAY	Digital CMOS VLSI Design **19MT15703**
26/05/2022 2:30 PM TO 4:30 PM	THURSDAY	IC Fabrication **19MT15705**
27/05/2022 2:30 PM TO 4:30 PM	FRIDAY	FPGA Architectures **19MT15707**
28/05/2022 2:30 PM TO 4:30 PM	SATURDAY	Research Methodology and IPR **19MT10708**

1. Students have to bring their College Identity Cards to the examination hall; otherwise they will not be permitted to write the examination.
2. Examination will be on the Units prescribed in the Syllabus Book.
3. College buses will leave the college with in 15 minutes after Examination Time.

PRINCIPAL

Copy to: 1) The Director, Academics & Research,SVEC.
2) The Vice-Principal, SVEC.
3) The Dean Academics, SVEC.
4) The Dean Placements &
5) The HOD of ECE : with a request to arrange to read out in the respective class rooms and circulation among the staff and to display on notice board.
6) The Examination Section.
7) The S.A.O, for information and necessary transport
8) Hostel Notice Boards
9) The office,ISA