Sree Vidyanikethan Engineering College (Autonomous)

Sree Sainath Nagar, A. Rangampet, Tirupati,Chittoor,Andhra Pradesh

I B.Tech II Semester (SVEC-20) Supplementary Examinations, January - 2023

TIME - TABLE

Date:03/01/2023

EXAM DATE & TIME	WEEK DAY	CE	CSD	CSBS	CSE	CSE (AI)	CSE (DS)	CSE (CS)	CSE (AI&ML)	CSE (IoT)	CSSE	ECE	EEE	EIE	IT	ME
30/01/2023 10:00 AM To 01:00 PM	MONDAY	Transformation Techniques and Linear Algebra 20BT2BS01	Transformation Techniques and Linear Algebra 20BT2BS01	Transformation Techniques and Linear Algebra 20BT2BS01	Transformation Techniques and Linear Algebra 20BT2BS01	Transformation Techniques and Linear Algebra 20BT2BS01	Transformation Techniques and Linear Algebra 20BT2BS01	Transformation Techniques and Linear Algebra 20BT2BS01	Transformation Techniques and Linear Algebra 20BT2BS01	Transformation Techniques and Linear Algebra 20BT2BS01	Transformation Techniques and Linear Algebra 20BT2BS01	Transformation Techniques and Linear Algebra 20BT2BS01	Transformation Techniques and Linear Algebra 20BT2BS01	Transformation Techniques and Linear Algebra 20BT2BS01	Transformation Techniques and Linear Algebra 20BT2BS01	Transformation Techniques and Linear Algebra 20BT2BS01
01/02/2023 10:00 AM To 01:00 PM	WEDNESDAY	Civil Engineering Materials and Concrete Technology 20BT20101	Engineering Physics 20BT1BS03	Engineering Physics 20BT1BS03	Engineering Physics 20BT1BS03	Engineering Chemistry 20BT1BS02	Engineering Chemistry 20BT1BS02	Engineering Physics 20BT1BS03	Engineering Chemistry 20BT1BS02	Engineering Physics 20BT1BS03	Engineering Physics 20BT1BS03	Engineering Chemistry 20BT1BS02	Engineering Chemistry 20BT1BS02	Engineering Chemistry 20BT1BS02	Engineering Physics 20BT1BS03	Applied Physics 20BT1BS04
03/02/2023 10:00 AM To 01:00 PM	FRIDAY	Basic Electrical and Electronics Engineering 20BT10201	Digital Logic Design 20BT20501	Basic Electrical and Electronics Engineering 20BT10201	Digital Logic Design 20BT20501	Digital Logic Design 20BT20501	Digital Logic Design 20BT20501	Digital Logic Design 20BT20501	Digital Logic Design 20BT20501	Digital Logic Design 20BT20501	Digital Logic Design 20BT20501	Network Analysis 20BT20241	Electrical Circuits 20BT20201	Network Analysis 20BT20241	Digital Logic Design 20BT20501	Basic Engineering Mechanics 20BT20301
06/02/2023 10:00 AM To 01:00 PM	MONDAY	Programming in C and Data Structures 20BT20541	Object Oriented Programming through Java 20BT21501	Object Oriented Programming through Java 20BT21501	Object Oriented Programming through Java 20BT21501	Object Oriented Programming through Java 20BT21501	Object Oriented Programming through Java 20BT21501	Object Oriented Programming through Java 20BT21501	Object Oriented Programming through Java 20BT21501	Object Oriented Programming through Java 20BT21501	Object Oriented Programming through Java 20BT21501	Programming in C and Data Structures 20BT20541	Programming in C and Data Structures 20BT20541	Programming in C and Data Structures 20BT20541	Object Oriented Programming through Java 20BT21501	Programming in C and Data Structures 20BT20541
08/02/2023 10:00 AM To 01:00 PM	WEDNESDAY	Communicative English 20BT1HS01	Communicative English 20BT1HS01	Data Structures and Algorithms 20BT22901	--	--	--	--	--	Communicative English 20BT1HS01	--	Communicative English 20BT1HS01	Communicative English 20BT1HS01	Communicative English 20BT1HS01	--	Communicative English 20BT1HS01

PRINCIPAL

Copy to : The Director, Academics and Research, SVEC.
The Vice-Principal, SVEC.
The Dean, Academics.
The Dean, Placements.
The HODs, of CE, EEE, ME, ECE, CSE, EIE, IT, CSSE and BS&H: with a request to arrange to read over in the respective class rooms and circulate among the staff members and display on notice Board.
The Examination Section.
The S.A.O, SVEC for information.
The Office, Valmar for necessary transport and dining arrangements.
The Vice President, Administration for information.